CLAIMS:

What is claimed is:

1. A method in a data processing system for accessing a memory, the method comprising:

verifying access rights for a memory operation using a first data structure in response to receiving a request to perform the operation, wherein the request includes a virtual address for the operation; and

responsive to access rights being verified for the memory operation, translating the virtual address into a real address using a second data structure.

2. The method of claim 1, wherein the first data structure is a first table and the second data structure is a second table.

3. The method of claim 2, wherein the first table is a protection table and the second table is an address translation table.

4. The method of claim 1, wherein the first data structure includes a virtual address of a start of a memory region within the memory for the operation.

5. The method of claim 4, wherein the first data structure includes a length of the memory region.

6. The method of claim 4, wherein the translating step includes:

subtracting the virtual address of a start of a memory region from the virtual address in the request to form a set of bits to access the second data structure.

7. The method of claim 6, wherein the set of bits includes lower order bits and higher order bits and wherein the higher order bits are used as an index into the second data structure and wherein the lower order bits are used as an index into a page in an entry in the second data structure.

8. A data processing system comprising:

a bus system;

a communications unit connected to the bus, wherein data is sent and received using the communications unit;

a memory connected to the bus system, wherein a set of instructions are located in the memory; and

a processor unit connected to the bus system, wherein the processor unit executes the set of instructions to verify access rights for a memory operation using a first data structure in response to receiving a request to perform the operation, wherein the request includes a virtual address for the operation; and translating the virtual address into a real address using a second data structure in response to access rights being verified for the memory operation.

9. The data processing system of claim 8, wherein the bus system includes a primary bus and a secondary bus.

10. The data processing system of claim 8, wherein the processor unit includes a single processor.

11. The data processing system of claim 8, wherein the processor unit includes a plurality of processors.

12. The data processing system claim 8, wherein the communications unit is an Ethernet adapter.

13. A data processing system for accessing a memory, the method comprising:

verifying means for verifying access rights for a memory operation using a first data structure in response to receiving a request to perform the operation, wherein the request includes a virtual address for the operation; and

translating means, responsive to access rights being verified for the memory operation, for translating the virtual address into a real address using a second data structure.

14. The data processing system of claim 13, wherein the first data structure is a first table and the second data structure is a second table.

15. The data processing system of claim 14, wherein the first table is a protection table and the second table is an address translation table.

16. The data processing system of claim 13, wherein the first data structure includes a virtual address of a

start of a memory region within the memory for the operation.

17. The data processing system of claim 16, wherein the first data structure includes a length of the memory region.

18. The data processing system of claim 16, wherein the translating means includes:

subtracting means for subtracting the virtual address of a start of a memory region from the virtual address in the request to form a set of bits to access the second data structure.

19. The data processing system of claim 18, wherein the set of bits includes lower order bits and higher order bits and wherein the higher order bits are used as an index into the second data structure and wherein the lower order bits are used as an index into a page in an entry in the second data structure.

20. A computer program product in a computer-readable medium for accessing a memory in a data processing system, the computer program product comprising:

first instructions for verifying access rights for a memory operation using a first data structure in response to receiving a request to perform the operation, wherein the request includes a virtual address for the operation; and

second instructions, responsive to access rights being verified for the memory operation, for translating

the virtual address into a real address using a second data structure.